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**Patent/TM/App/Serial #** 10, 733, 216

**Program Area** Publishing

**Date Processed** 10-28-05

**ATTENTION ATTENTION ATTENTION**

SEP 13 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE, 2005 SEP 16 10 10 25

Patentee: Kuo-Chi Tu, et al.

Patent No.: 6,833,578

Issue Date: December 21, 2004

Entitled: Method and Structure Improving  
Isolation Between Memory Cell  
Passing Gate and CapacitorDocket No.: 24061.46 US PATENT & TRADEMARK  
OFFICE

Serial No.: 10/733,216

Filing Date: December 11, 2003

VIA FACSIMILE - 703-305-8568

Mail Stop PGFUB

Commissioner for Patents

PO Box 1450

Alexandria, VA 22313-1450

REQUEST FOR REFUND OF PRE-GRANT PUBLICATION FEE

Dear Sir:

Patentee hereby requests refund of the pre-grant publication fee timely paid on November 10, 2004. A copy of Issue Fee Transmittal, indicating payment of publication fee and return postcard is enclosed herewith.

According to the Updated Filing Receipt (copy enclosed) the pre-grant publication was scheduled to publish on June 16, 2005. Patentee notes that the subject application proceeded to allowance and issued prior to the projected publication date. It has been more than four weeks since the issue date and therefore, refund of the publication fee under 37 CFR 1.18(d) is respectfully requested.

Patentee respectfully requests that a refund of \$300.00 be credited to the Deposit Account of Haynes and Boone, LLP Number 08-1394. This form submitted in duplicate.

Respectfully submitted,


David M. O'Dell  
Registration No. 42,044

Date: 9-13-05

HAYNES AND BOONE, LLP  
901 Main Street, Suite 3100  
Dallas, Texas 75202-3789  
Telephone: 972-739-8635  
Facsimile: 214-200-0853

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SEP 13 2005

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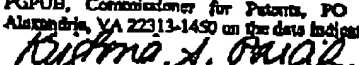
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APPL NO.	FILING OR 371 (a) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/733,218	12/11/2003	2818	918	24061.46 (TSMC2003-0009)	5	21	3

David M. O'Dell  
Attorney for Applicants  
Haynes and Boone, LLP  
901 Main Street, Suite 3100  
Dallas, TX 75202-3789

CONFIRMATION NO. 8902

UPDATED FILING RECEIPT

  
"C000000012391303"

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HAYNES and BOONE, LLP  
RICHARDSON

Date Mailed: 04/19/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-748-8195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

Kuo-Chi Tu, Hsin-Chu, TAIWAN;  
Chun-Yao Chen, Hsin-Chu, TAIWAN;  
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Chung-Wei Chang, Hsin-Chu, TAIWAN;  
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Tsung-Hsun Huang, Taipei County, TAIWAN;  
Hsiao-Hui Tseng, Tainan City, TAIWAN;

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APR 21 2004

HAYNES &amp; BOONE LLP

## Assignment For Published Patent Application

Taiwan Semiconductor Manufacturing Co., Ltd., Hsin-Chu, TAIWAN;

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 03/17/2004

Projected Publication Date: 06/16/2005

Non-Publication Request: No

12.11.04-DD to FF  
2.11.05- awaiting OA

Docketed 4.21.04

By ref  
TB/DH

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Early Publication Request: No

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## Title

Method and structure improving isolation between memory cell passing gate and capacitor

## Preliminary Class

365

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**Title 37, Code of Federal Regulations, 5.11 & 5.15**

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Romie Boyle  
11-10-04

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,216	12/11/2003	Kuo-Chi Tu	24061.46	8002

TITLE OF INVENTION: METHOD AND STRUCTURE IMPROVING ISOLATION BETWEEN MEMORY CELL PASSING GATE AND CAPACITOR

APPL. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	12/20/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
HO, TU, TV, V	2818	257-301000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" Indication (or "Fee Address" Indication form PTO/SB/47; Rev. 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent from page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 3 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Haynes and Boone, LLP

2. \_\_\_\_\_

3. \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 1.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Taiwan Semiconductor Manufacturing Company, Ltd. Hsin-Chu, Taiwan R. O. C.

(B) RESIDENCE (CITY AND STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
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5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(e)(2).

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Authorized Signature

David M. O'Dell

Typed or printed name

Date 11-10-04

Registration No. 62,046

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OMB 0651-0033 U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

PAGE 5/6 \* RCVD AT 9/13/2005 4:50:37 PM [Eastern Daylight Time] \* SVR:USPTO-EFRRF-6/29 \* DNIS:2738300 \* CSID: \* DURATION (mm:ss):01:42

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HAYNES & BOONE LLP.			
APPLICANT	Tu et al.		
SERIAL NO.	10/733216	DATE FILED	12/11/2003
ATTORNEY DOCKET NO.	24061.46		
TITLE	Method and Structure Improving Isolation Between Memory Cell Passing Gate and Capacitor		
SENDER'S INITIALS	DMO/lat/beb	DATE MAILED	11-10-04

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